REMARKS/ARGUMENTS

The applicants' attorneys appreciate the Examiner's thorough search and remarks.

Responsive to the objections against the specification, the limitation "a free surface" has been amended out of claim 1. Withdrawal of the objections is requested.

Responsive to the remaining objections, source regions 10 are an example of conductive regions of first conductivity adjacent the MOS-gated structure and drain contact 22 is an example of an electrical contact as set forth in claim 1. It is respectfully submitted that the examples set forth in the specification adequately support claim 1. Reconsideration is requested.

Claims 1 and 6 have been combined.

Claim 6 was rejected as obvious over the background of the application in view of Frisina, U.S. Patent No. 6,586,798. Reconsideration is requested.

It has been asserted that the prior art as set forth in the background of the application, includes the following:

> growing epitaxially a second semiconductor layer 18" of said first conductivity N over said first semiconductor layer 18 of said first conductivity refer to Background of Invention;
>
> forming a second mask [0015] over a free surface of said second semiconductor layer, said second mask including a plurality of windows exposing portions of said second semiconductor layer, and being capable of blocking implants; and performing a series of implants through said implant windows in said second mask to form a plurality of vertically adjacent regions of said second conductivity in said second semiconductor layer below said implant windows and above said vertically oriented regions 28 of said second conductivity in said first semiconductor layer.

The present invention is concerned with a method for manufacturing a power semiconductor device which has incorporated in the body thereof a superjunction structure. A superjunction structure typically includes bodies of opposite conductivity in substantial charge balance that deplete one another under reverse bias conditions allowing for improvement in breakdown voltage without having to compromise on resistance (Rdson). A conventional superjunction structure, for example, in N-channel power MOSFETs includes P columns formed in an N-type drift region. Figure 2 illustrates such a prior art structure. In the structure shown in

Figure 2, the P columns 28 are formed by a method which includes forming an epitaxial silicon layer of one conductivity, implanting only once to form regions of a second conductivity, forming a second epitaxial layer of the one conductivity over the first epitaxial layer, implanting again once to form regions of the second conductivity, continuing the process until the desired thickness is reached, and thereafter applying a diffusion step to link up the regions of the second conductivity. See specification at page 4, lines 3-15.

This prior art method, which involves a single implant per each epitaxial layer, limits the cell pitch size. See page 4, lines 14-19.

In a method according to the present invention the cell pitch can be improved. Specifically, by using multiple, closely spaced implants in each epitaxial layer instead of the single implants of the prior art, the implanted regions are not required to be diffused far distances in order to link up vertically. Therefore, the lateral dimension of the implanted regions can be kept close to the width of the implant windows. Given that implant windows can be formed to be very narrow, narrow columns of the second conductivity can be formed in the drift region of the device, thereby reducing the cell pitch. The prior art as explained in the background does not show or suggest the steps as set forth in claim 1. Reconsideration is requested.

Claims 2-17 depend from claim 1. Each of these dependent claims includes limitations, which in combination with those of claim 1 are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 3, 2005:

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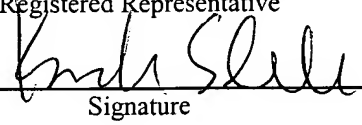

Signature

March 3, 2005
Date of Signature

Respectfully submitted,

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